



JUNE 23-27, 2024

MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA



Considering selective resistance extraction for performance & accuracy trade-off for memory IP simulation

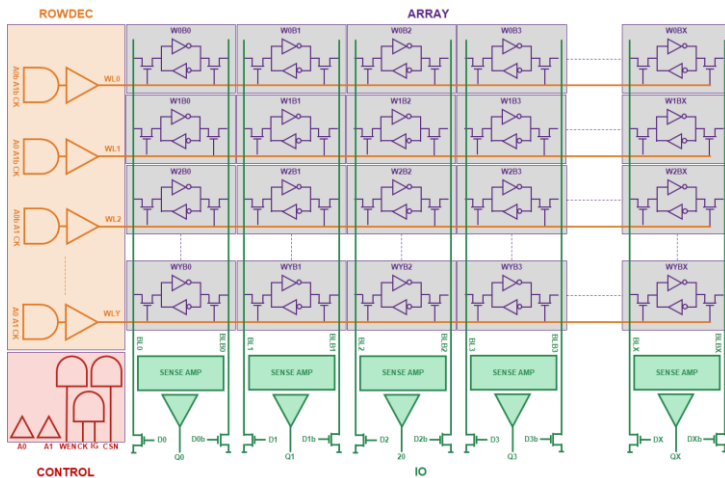
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²Synopsys



Motivation: simulation challenges in memory



Basic SRAM architecture

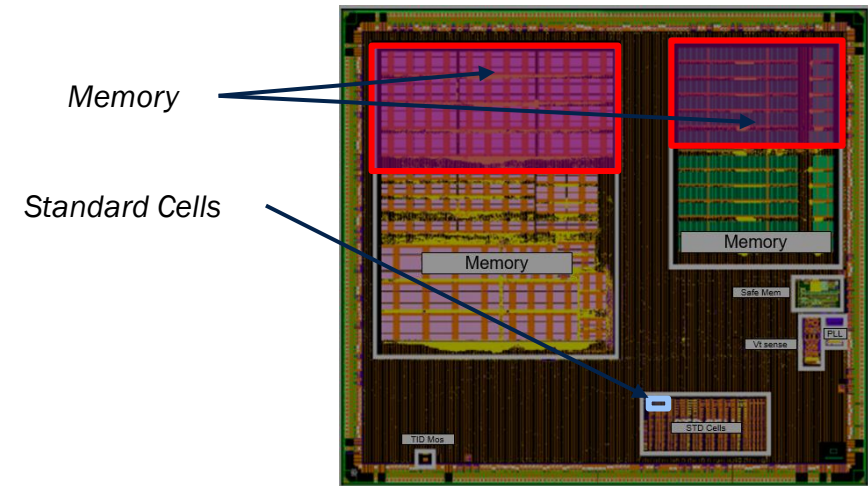
Redundancy	Safety	Debug
Bit Mask	Bypass	Scan modes

Functional behavior options

Words	Bits	Vt flavors	Voltage
Mux	Bank	Process	Temperature

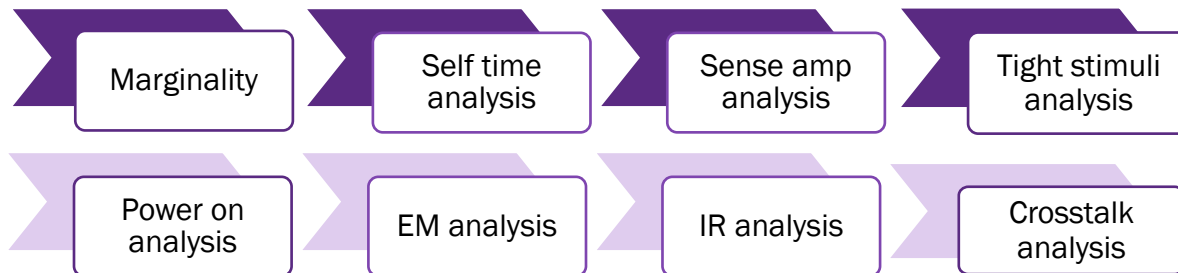
Physical parameters

Operating variations

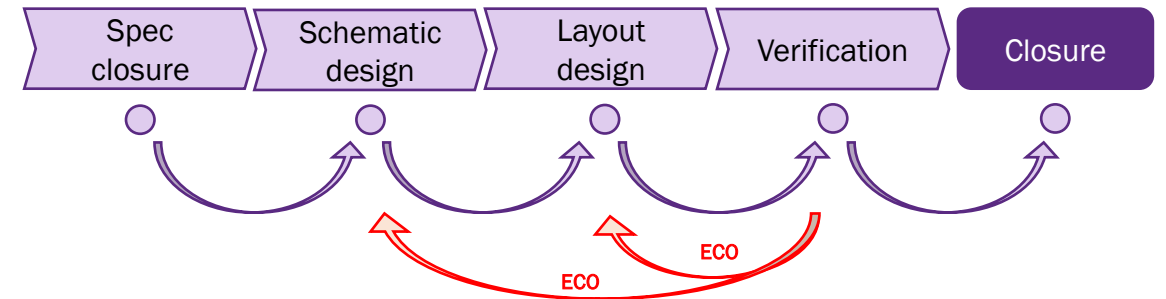


Sample floorplan of SOC

Memory IP are very large compared to any other Custom IP with many options and features to serve many applications

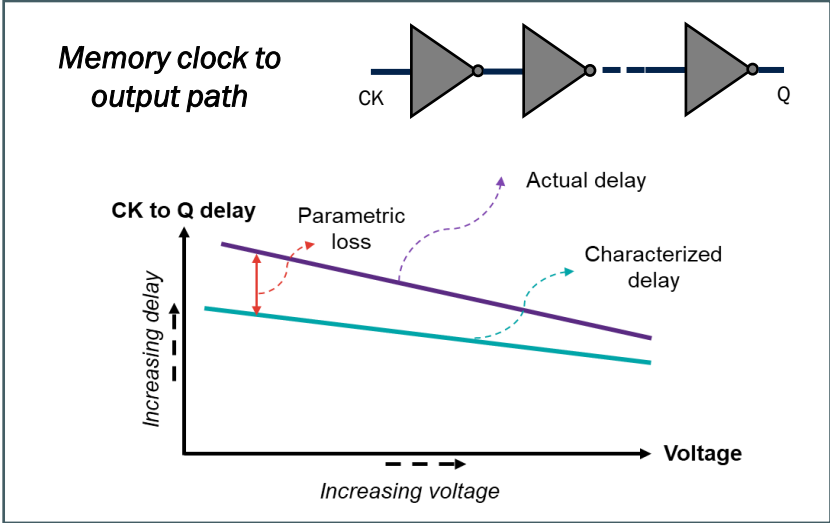


Some verification steps in memory design



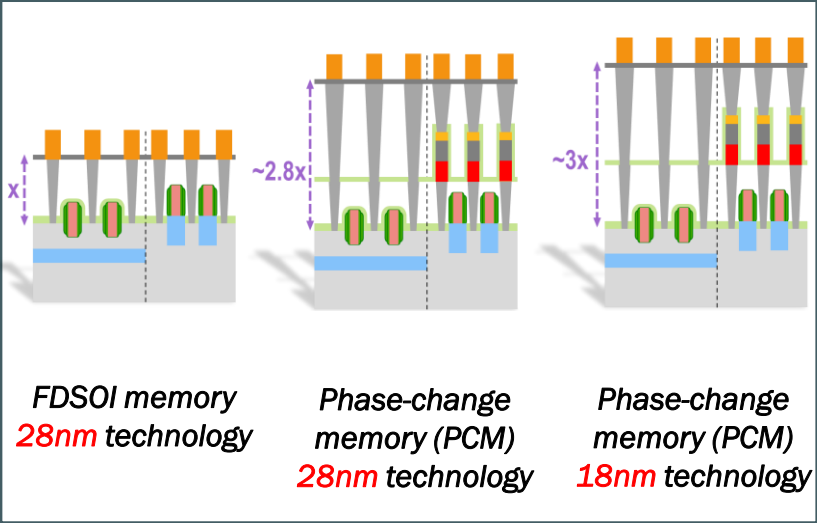
Design verification involves many complex steps, which often result in ECOs (re-layouting). Simulations for such verifications, covering all combinations, are extensive and necessary to meet timing, power and leakage specifications.

Impact of contact resistance increase on delay, margins and IR drop



Parametric loss in characterized delay due to voltage drop

Memory design requires extracted (post-layout) views, and any wrong modelling of power-net RCs can result in wrong timing (due to wrong IR Drop considerations)



Contact height dominance with advancement in technology

As technology shrinks, the height of contact increases and hence the contact resistance. This dominates power network R and hence dominates IR drop & delay

Contact	Typical Resistance		
	FDSOI 28nm technology	PCM 28nm technology	PCM 18nm technology
CA n+/p+ on RX	X	1.6*X	3.3*X
CA n+/p+ on PC	Y	1.7*Y	2.0*Y

Increase in resistance leading to voltage drop in lower technology

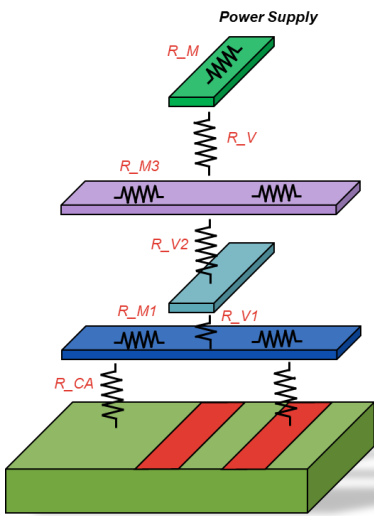
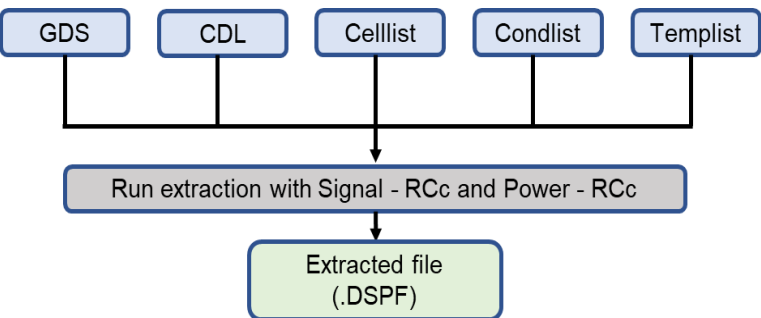
Furthermore, to quantify the increase in contact resistance (in FD-SOI technologies), contact resistance increases by 3.3X when moving from 28 nm to 18 nm

These complexities highlight the importance of considering power-net RCs in design verification which could otherwise lead to functional loss and yield loss.

Accurate extraction methodology vs current methodology

Accurate methodology

RCc is extracted for both power and signal



$\{R_{M1}, R_{M2}, \dots R_M\}$

$\{R_{V1}, R_{V2}, \dots R_V\}$

$\{R_{CA}\}$

Considered for power supply lines

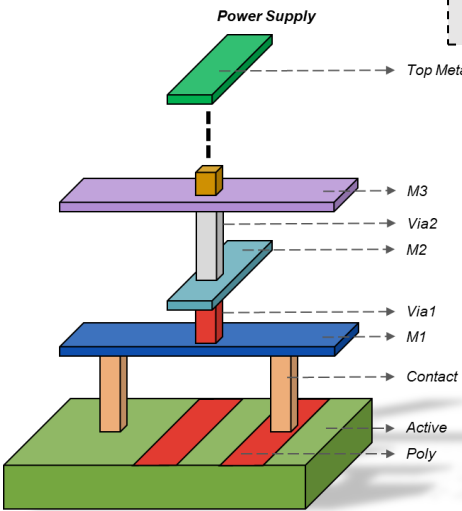
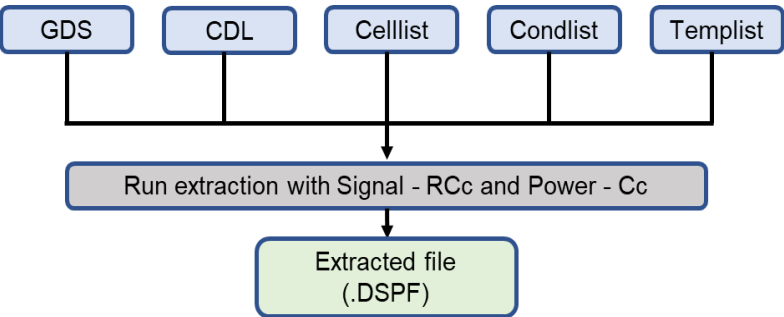


Accounts interconnect resistance for power supply lines

Note: Cc has lesser impact on simulation runtime and is always considered for both power and signal nets.

Current methodology

RCc is extracted for signals while Cc is extracted for power

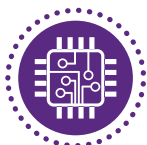


$\{R_{M1}, R_{M2}, \dots R_M\}$

$\{R_{V1}, R_{V2}, \dots R_V\}$

$\{R_{CA}\}$

Not considered for power supply lines



Size of extracted file (DSPF) is compact

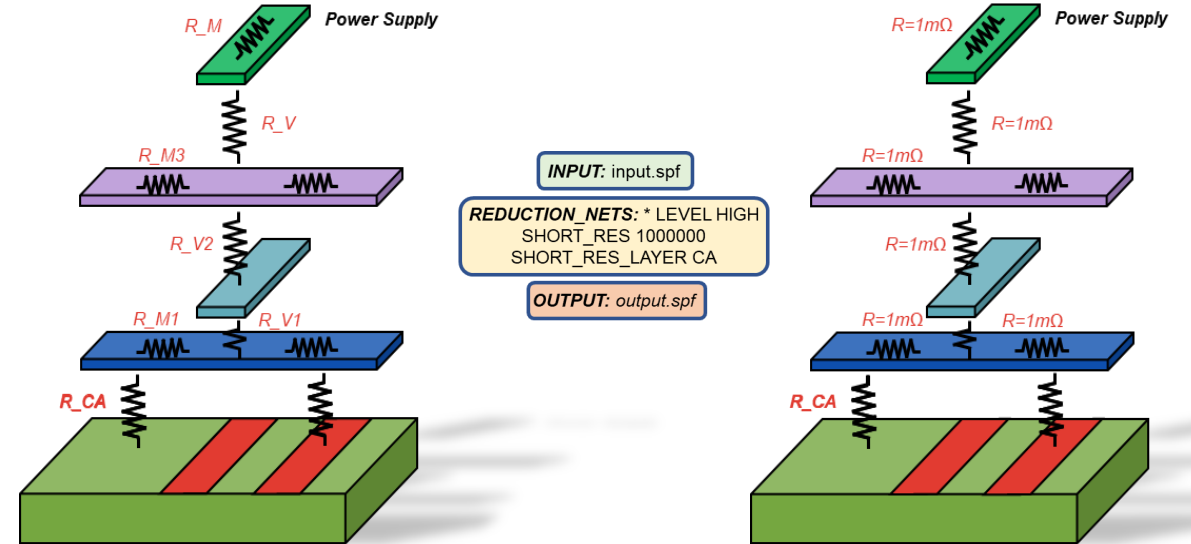
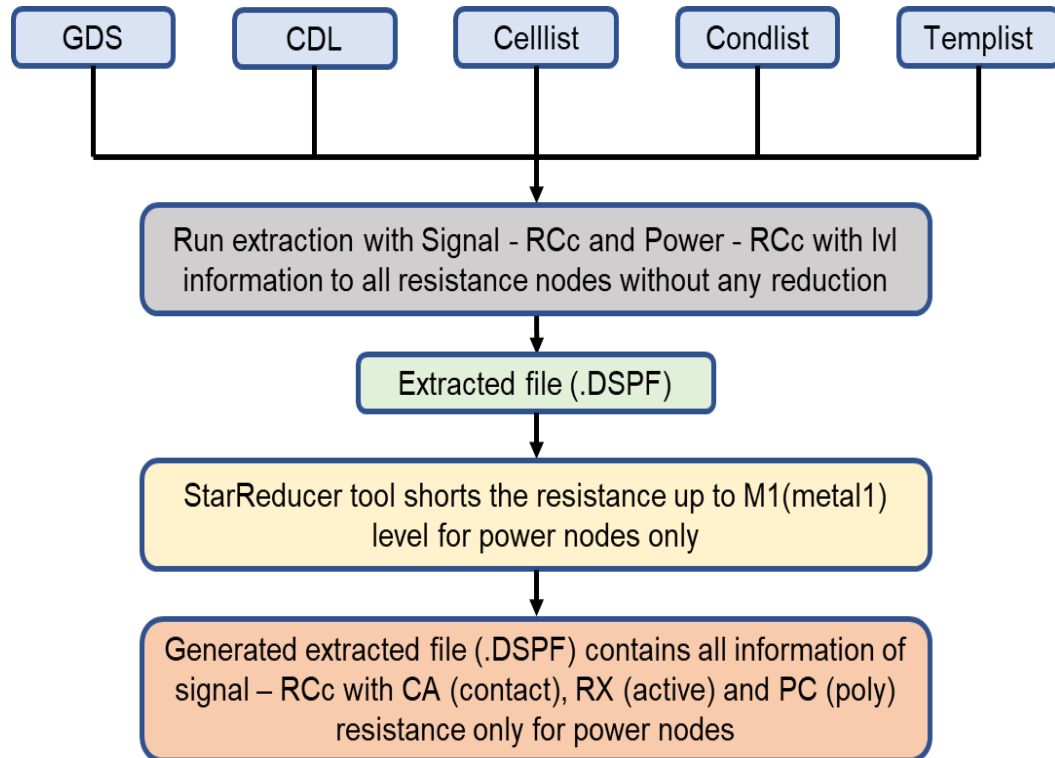


Runtime of simulations is less



Ease in design verification and analysis

Proposed extraction methodology



Standalone Reducer Tool is used to perform layer-based extraction

- Contact resistance is dominating the power net RCs, so we keep only contact R and ignore all other metal R in the power net
- Standalone reducer tool like StarReducer from StarRC is used. StarReducer is run on DSPF file dumped from extraction tool like StarRC
- It gives us flexibility to do Net based, R/C based and layer-based reductions as required

Comparison of results and summary

Case	Delay (in ps)		Percentage diff. (wrt Accurate methodology)		Case	DSPF file size	Simulation run time	Accuracy
	CK to DWL	SENO to Q	CK to DWL	SENO to Q				
Accurate methodology	197	38.6	0%	0%	Accurate methodology	1X	1X	Accurate
Current methodology	188.2	37.1	-4.4%	-3.8%	Current methodology	0.3X	0.2X	Less Accurate
Proposed methodology	194.8	38.3	-1.1%	-0.7%	Proposed methodology	0.43X	0.25X	Closer to Accurate

*CK to DWL: Clock to Dummy Word-line delay
 *SENO to Q: Sense-Amp Output to Output delay

- **Current methodology** is less accurate for technologies like
 - Delay ~4% faster (optimistic) in critical delays with respect to accurate method
 - Multiple iterations for design closure or yield loss
- For **accurate methodology** runtime increased by 5X due to increased DSPF file size
- **Proposed methodology** is more accurate and runtime overhead was just 5%

Conclusion

- Proposed methodology ensures improved robustness (yield) with minimal impact on simulation runtime
- It reduces iterations for delay, margin and IR drop closure in design cycle having no overhead while implementation



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Thank you!

